INTEGRATED CIRCUIT FAULT INSERTION SYSTEM

ABSTRACT OF THE INVENTION

A system for fault insertion in an integrated circuit that resides in a functional portion of the integrated circuit. The fault insertion system is controlled through a Fault Control Register, comprising a Fault Identification Register (FIR), and a Fault Apply Register (FAR). The FIR is connected to a FIR decode block which, depending on the values contained in the FIR, applies signals to one or more node fault logic blocks. The node fault logic blocks either apply a test signal to a circuit node, or apply the normal system signals to the node. The FAR controls an enable signal to the FIR decode block, and determines when, and the duration, that the test signal will be applied. An External Control Bit of the FAR also allows manual control of the test signal.